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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,508	06/06/2000	Guy Lynn Guthrie	AT9-99-505	8141

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BRACEWELL & PATTERSON LLP
PO BOX 969
AUSTIN, TX 78767-0969

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/588,508	Applicant(s) GUTHRIE ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been considered. Claims 1, 3, 5, 7, 9, and 10 have been amended as part Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 5-6, and 9 are rejected under 35 U.S.C. 102(e) as being taught by Sproull, U.S. Patent Number 6,038,646 (herein referred to as Sproull).

4. Referring to claim 1, Sproull has taught a data processing system comprising:

   a. An interconnect (Sproull column 6, lines 25-43; column 7, 46-50; Figure 1 and Figure 2);

   b. An in-order processor that issues all memory access requests in program order (Sproull column 2, lines 56-63; column 3, lines 10-54; column 5, line 39 to column 6, line 20), wherein said processor issues said memory access requests from an instruction sequence only in said program order and accepts data retrieved by a first and a second memory access request into its execution units only in said program order (Sproull column 5, line 39 to column 6, line 20; Figure 1; and Figure 2);

c. A memory system coupled to said processor which supports completing memory access requests in a weakly consistent order (Sproull column 6, lines 25-43; Figure 1; and Figure 2); and

d. A controller associated with said processor that forwards said memory access requests to said memory system (Sproull column 4, line 52 to column 5, line 12; column 7, lines 36-50; and Figure 2) and which automatically places a barrier operation on said interconnect following each issuance of a memory access request to said memory system (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b), wherein said barrier operation indicates a need to complete the data operations associated with the memory access requests in program order from the perspective of the processor (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b).

5. Referring to claim 2, Sproull has taught wherein said controller includes means for creating said barrier operations (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b).

6. Referring to claim 5, Sproull has taught an in-order processor comprising:

a. An instruction sequencing unit (ISU) that receives memory access instructions in program order (Sproull column 2, lines 56-63; column 3, lines 10-54; column 5, line 39 to column 6, line 20);

b. A load store unit (LSU) including a controller that issues memory access requests associated with said memory access instructions to an interconnect that couples said processor to a memory system (Sproull column 6, lines 25-43; column 7, 46-50; Figure 1 and Figure 2) and wherein said controller automatically places a barrier operation on said interconnect in response to each issuance of a memory access request (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b), wherein all said memory access requests are forwarded to memory in the program order (Sproull column 5, line 39 to column 6, line 20; Figure 1; and Figure 2).

7. Referring to claim 6, Sproull has taught wherein said controller includes means for creating said barrier operations (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b).

8. Referring to claim 9, Sproull has taught a method of processing instructions in a data processing system, having a memory system (Sproull column 6, lines 25-43; column 7, 46-50; Figure 1 and Figure 2), said method comprising the steps of:

a. Receiving an instruction sequence at a processor in program order, said instruction sequence including at least a first and a second memory access instruction (Sproull column 2, lines 56-63; column 3, lines 10-54; column 5, line 39 to column 6, line 20; Figure 1; and Figure 2;

b. In response to receipt of said memory access instruction, generating a memory access request and a barrier operation (Sproull column 3, line 55 to column 4, line

3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b);

c. Automatically initiating said barrier operation after said memory access request is issued to a memory system (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b); and

d. Upon completion of said barrier operation, completing said first and said second memory access request in program order at said processor (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-4, 7-8, and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sproull, U.S. Patent Number 6,038,646 (herein referred to as Sproull) as applied to claims 1, 5, and 9 above, in view of Karp et al., U.S. Patent Number 6,321,328 (herein referred to as Karp).

11. Referring to claims 3, 7, and 10, Sproull has taught

a. Means for ignoring a pending barrier operation when a subsequent load request appears in the instruction sequence (Applicant's claims 3, 7) (Sproull column 3,

line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b); and

b. Ignoring a pending barrier operation of said first memory access request when a subsequent memory access request in the instruction sequence is a load request (Applicant's claim 10) (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b).

12. Sproull has not explicitly taught speculatively issuing load requests to said memory system and interconnect before the pending instruction is completed, wherein said subsequent load request is speculative because said subsequent load request is issued before a previous memory access request that may invalidate or change data retrieved by said load request completes within the memory system (Applicant's claims 3, 7, and 10). However, Sproull has taught issuing the subsequent load requests to said memory system and interconnect (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b). A person of ordinary skill in the art at the time the invention was made, and as taught in Karp, that speculative issuing of load instructions improves memory latency and ensures that data that is currently needed for execution is not displaced (Karp column 1, lines 41-60 and columns 1-2, lines 66-18), thereby increasing a processor's efficiency by decreasing memory latency associated with fetching data from memory (Karp column 1, lines 11-20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the speculatively issued load

instruction of Karp in the device of Morris to decrease memory latency and increase processor speed.

13. Referring to claims 4, 8, and 11, Sproull has taught

a. Wherein said controller includes means for allowing data returned by a speculatively issued load request to be utilized by said processor only when an acknowledgment is received from all barrier operations pending when said load was issued (Applicant's claims 4 and 8) (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b); and

b. The step of forwarding data returned by said speculatively issued load request to a register or execution unit of said processor, when an acknowledgment is received for said barrier operation (Applicant's claim 11) (Sproull column 3, line 55 to column 4, line 3; column 4, line 52 to column 5, line 12; column 8, line 8 to column 9, line 34; Figure 3a; and Figure 3b).

Response to Arguments

14. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aimee J. Li
April 13, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100